B1 end

forming a first trench into a semiconductor substrate;

forming a dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench;

forming a second trench into said substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;

forming an insulative material in said first and second trenches at least partially by substantially consuming said spacer and said dielectric lining to substantially fill said first and second trenches with said insulative material.

Sub D2

26. (Amended) The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

B2 Contd

34. (Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

Sub C3

forming a first trench into a semiconductor substrate;

forming a dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench;

forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;

forming an insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said dielectric lining during formation to substantially fill said first and second trenches with said insulative material;

planarizing said insulative material;

wherein said process uses only one mask to form said device isolation.

B2 Sub D5 end

35. (Amended) The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

B3

40. (Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

Sub C5

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;

forming an oxide filler in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

Sub D8

41. (Amended) The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

B4 Contd

50. (Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

Sub C6

forming a trench into a semiconductor substrate;

forming a dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench;